WHAT IS CLAIMED IS:

1. A method for constructing at least one digital input signal and providing at least one analog representation signal thereof, comprising:
   (a) feeding a DSP with said at least one digital input signal and a synchronization clock,
   (b) repeatedly identifying a model of a constructing device for creating a representation of the relationships between said DSP digital outputs and at least one of said at least one analog representation signal of said constructing device, wherein said constructing device comprising discrete output devices and a MIMO system,
   (c) said DSP is calculating n digital outputs, by using said at least one digital input signal and the identified model of said constructing device,
   (d) said n digital outputs are received by k discrete output devices comprising, in total, n digital inputs, m analog outputs, and simple conversion rules between said n digital inputs and said m analog outputs,
   (e) said MIMO system receiving said m analog outputs, and providing at least one output analog signal equivalent to said al least one digital input signal.
2. The method of claim 1, wherein said MIMO system is constructed from low accuracy components featuring high bandwidth, high gain, and low current consumption.
3. The method of claim 1, wherein said model incorporates and compensated for most of the noise created by the digital input signals constructor of the present invention, contaminating the digital input signal or the intermediate signals.
4. The method of claim 1, wherein said model incorporates and compensated for clock skew.
5. The method of claim 1, wherein said MIMO system is time varying according to said synchronization clock.

6. The method of claim 1, wherein said identifying comprising identify the inverse relation.

7. The method of claim 1, wherein said identifying a model comprising feeding at least one known digital signal to said at least one digital input signal in a training period, and reading said known digital signal and digital result from at least one ADC connected to said at least one analog representation signal, and identifying the model of said constructing device by applying a system identification algorithm.

8. The method of claim 7, wherein said at least one known digital signal comprising a sequence of independently and identically uniformly distributed pseudo-random numbers.

9. The method of claim 1, wherein said model is identified by applying an identification algorithm that is using an a-priori statistical knowledge.

10. The method of claim 1, wherein said constructing device is enclosed in a system performing several signal processing functions which contains information regarding said at least one analog representation signal, and said information is sufficient for enabling an identification algorithm of the model constructing device.

11. The method of claim 1, wherein an additional signal constructor comprising a system model with unknown parameters is used for identifying said model of a constructing device, and unknown parameters of both models are identified by joint model identification algorithm.

12. The method of claim 11 where said joint model identification algorithm is based on feeding said constructing device with at least one known training sequence.

13. The method of claim 12, wherein said at least one known training sequence comprising an independently and identically distributed pseudo-random sequence.

14. The method of claim 1, wherein said identifying a model comprising low speed components sampling said at least one analog representation signal every few samples and training only on the sampled samples.

15. The method of claim 1, wherein said identifying a model comprising a

low speed DAC reference, wherein a training digital signal is fed both to said low speed DAC reference and to said constructing device, and the analog output signals of low speed DAC reference and said at least one analog representation signal are subtracted in order to create an error signal; said error signal is sampled and fed to said DSP for training.

16. The method of claim 1, wherein said discrete output devices comprising at least one low resolution digital to analog converter.

17. The method of claim 1, wherein the value of each of said m analog outputs is selected from a predefined group of values.

18. The method of claim 1, wherein said m analog outputs are time varying according to a predetermined waveform.

19. The method of claim 1, wherein said MIMO system is selected from the group consisting of continuous MIMO system, and MIMO system having a unified model, and continuous MIMO system having a unified model.

20. The method of claim 1, wherein said calculating n digital outputs is by inverting said model by using internal controller in order to keep the error to be within a deterministic or probabilistic set of predefined constraints and internal constructing device for implementing, in the digital domain, the mathematical equivalence of the transfer function of said constructing device.

21. The method of claim 19, wherein said MIMO system is a linear MIMO system.

22. The method of claim 1, wherein said constructing at least one digital input signal and providing at least one analog representation signal thereof comprising:

(a) at least one additional DSP, k discrete output devices, and MIMO system having a model, being fed by said at least one digital input signal and said synchronization clock,

(b) identifying said model of said MIMO system and said additional MIMO system by applying joint model identification algorithm.

23. The method of claim 1, wherein said at least one digital input signal providing at least one analog representation signal thereof is

implemented as a multi-stage configuration.

24. The method of claim 1, wherein said at least one digital input signal providing at least one analog representation signal thereof is implemented as a multi-stage configuration and said multi-stage configuration comprising an iterative control; said iterative control is transferring a residual error to subsequent stages in each stage where the control function is successfully implemented

25. The method of claim 1, wherein said at least one digital input signal providing at least one analog representation signal thereof is implemented as a feedback iterative configuration.

26. The method of claim 1, wherein said MIMO system is a linear MIMO system, and said identifying said model of said at least one digital input signal providing at least one analog representation signal thereof comprising LMS technique.

27. The method of claim 1, wherein said MIMO system receives said synchronization clock used for timing

28. A method for constructing at least one digital input signal and providing analog representation thereof, comprising:

(a) feeding a DSP with at least one digital input signal and synchronization clock,

(b) occasionally or within a repetitive training period, said DSP is identifying a model of at least one discrete output device and m MIMO stages, referred to as constructing device, for creating a representation of the relationships between digital outputs of said DSP and at least one analog output signals of m MIMO stages,

(c) calculating n digital outputs, by using said at least one digital input signal and the identified model of said constructing device,

(d) said n digital outputs are received by said at least one discrete output device comprising, in total, n digital inputs, m analog outputs, and simple conversion rules between said n digital inputs and said m analog outputs,

(e) corresponding MIMO stage to each one of said m analog outputs,

excluding first MIMO stage, are receiving at least one analog input signal from the preceding stage and the appropriate analog signal said at least one discrete output device; first MIMO stage is receiving only the appropriate analog signal from said at least one discrete output device; all m MIMO stages are providing at least one output analog signal; last MIMO stage is providing at least one output analog signal equivalent to said digital input signal.

29. The method of claim 28, wherein each of said m MIMO stages comprising attenuating the signal, and adding a predefined constant or subtracting said predefined constant from said attenuated signal, according to said DSP decision.

30. The method of claim 28, wherein said calculating n digital outputs is by inverting said model by using internal controller in order to keep the error to be within a deterministic or probabilistic set of predefined constraints and internal constructing device for implementing, in the digital domain, the mathematical equivalence of the transfer function of said constructing device.

31. The method of claim 30, wherein said calculating n digital outputs comprising: computing ISI terms, adding or subtracting said ISI terms from said digital input signal.

32. The method of claim 30, wherein said MIMO system is time varying according to said synchronization clock.

33. The method of claim 28, wherein said model is identified by applying an identification algorithm that is using an a-priori statistical knowledge.

34. The method of claim 28, wherein said constructing device is enclosed in a system performing several signal processing functions which contains information regarding said analog representation signal, and said information is sufficient for enabling an identification algorithm of the model constructing device.

35. The method of claim 28, wherein an additional signal constructor comprising a system model with unknown parameters is used for identifying said model of a constructing device, and unknown parameters

of both models are identified by joint model identification algorithm, and said joint model identification algorithm is based on feeding said constructing device with at least one known training sequence.

36. The method of claim 28, wherein said identifying a model comprising low speed components sampling said at least one analog representation signal every few samples and training only on the sampled samples.

37. The method of claim 28, wherein said calculating n digital outputs is by inverting said model by using internal controller in order to keep the error to be within a deterministic or probabilistic set of predefined constraints and internal constructing device for implementing, in the digital domain, the mathematical equivalence of the transfer function of said constructing device.

38. The method of claim 28, wherein said MIMO system is a linear MIMO system.

39. The method of claim 28, wherein said constructing at least one digital input signal and providing analog representation thereof comprising:

(a) at least one additional DSP, k discrete output devices, and MIMO system having a model, being fed by said at least one digital input signal and said synchronization clock,

(b) identifying said model of said MIMO system and said additional MIMO system by applying joint model identification algorithm.

40. The method of claim 28, wherein said at least one digital input signal providing at least one analog representation signal thereof is implemented as a multi-stage configuration.

41. The method of claim 28, wherein said at least one digital input signal providing at least one analog representation signal thereof is implemented as a multi-stage configuration and said multi-stage configuration comprising an iterative control; said iterative control is transferring a residual error to subsequent stages in each stage where the control function is successfully implemented

42. The method of claim 28, wherein said at least one digital input signal providing at least one analog representation signal thereof is

implemented as a feedback iterative configuration.

43. The method of claim 28, wherein said MIMO system is a linear MIMO system, and said identifying said model of said at least one digital input signal providing said analog representation thereof comprising LMS technique.

44. A device for constructing at least one digital input signal and providing analog representation thereof, comprising:

(a) A DSP fed with at least one digital input signal and synchronization clock,

(b) said DSP, occasionally or within a repetitive training period, is identifying a model of at least one discrete output device and m MIMO stages, referred to as constructing device, for creating a representation of the relationships between digital outputs of said DSP and at least one analog output signals of m MIMO stages,

(c) said DSP is calculating n digital outputs, by using said at least one digital input signal and the identified model of said constructing device,

(d) said n digital outputs are received by said at least one discrete output device comprising, in total, n digital inputs, m analog outputs, and simple conversion rules between said n digital inputs and said m analog outputs,

(e) corresponding MIMO stage to each one of said m analog outputs, excluding first MIMO stage, are receiving at least one analog input signal from the preceding stage and the appropriate analog signal said at least one discrete output device; first MIMO stage is receiving only the appropriate analog signal from said at least one discrete output device; all m MIMO stages are providing at least one output analog signal; last MIMO stage is providing at least one output analog signal equivalent to said digital input signal.

45. The device of claim 44, wherein said analog representation having RMS below 10 mili volt at frequency above 10 MHz.

46. The device of claim 44, wherein said model incorporates and

compensated for most of the noise created by the digital input signals device of the present invention, contaminating the digital input signal or the intermediate signals.

47. The device of claim 44, wherein said synchronization clock is a signal selected from the group consisting of fixed pulse shape and frequency, and any deterministic signal featuring frequency.

48. The device of claim 44, wherein said identifying comprising identify the inverse relation.

49. The device of claim 44, wherein said DSP is identifying a model comprising a training generator feeding at least one known digital signal to said at least one digital input signal in a training period, and reading said known digital signal and digital result from at least one ADC connected to said at least one analog representation signal, and identifying the model of said constructing device by applying a system identification algorithm.

50. The device of claim 49, wherein said at least one known digital signal comprising a sequence of independently and identically uniformly distributed pseudo-random numbers.

51. The device of claim 49, wherein said DSP is implemented by two separate DSPs

52. The device of claim 49, wherein said training generator is implemented within said DSP.

53. The device of claim 44, wherein said model is identified by applying an identification algorithm that is using an a-priori statistical knowledge.

54. The device of claim 44, wherein said constructing device is enclosed in a system performing several signal processing functions which contains information regarding said at least one analog representation signal, and said information is sufficient for enabling an identification algorithm of the model constructing device.

55. The device of claim 44, wherein an additional signal constructor comprising a system model with unknown parameters is used for identifying said model of a constructing device, and unknown parameters

of both models are identified by joint model identification algorithm.

56. The device of claim 44, wherein said identifying a model comprising low speed components sampling said at least one output analog signal every few samples and training only on the sampled samples.

57. The device of claim 44, wherein said discrete output devices comprising at least one low resolution digital to analog converter.

58. The device of claim 44, wherein said MIMO system is selected from the group consisting of continuous MIMO system, and MIMO system having a unified model, and continuous MIMO system having a unified model.

59. The device of claim 58, wherein said MIMO system is a linear MIMO system.

60. The device of claim 44, wherein said device is implemented as a multi-stage configuration.

61. The device of claim 44, wherein said device is implemented as a multi-stage configuration and said multi-stage configuration comprising an iterative control; said iterative control is transferring a residual error to subsequent stages in each stage where the control function is successfully implemented

62. A multi-stage digital signals constructor, wherein each stage comprising:
   (a) amplifier amplifying an input digital signal,
   (b) means for approximately integrating the amplified digital signal,
   (c) means for synchronizing said multi-stage digital signals constructor,
   (d) means for adding at least one predefined correction to said amplified digital signal.

63. The device of claim 62, wherein said analog output signal having RMS below 10 mili volt at frequency above 10 MHz.

64. The device of claim 62, wherein said amplifier is open loop transconductance amplifier.

65. The device of claim 62, wherein said means for synchronizing comprises switching amplifier according to a clock.

66. The method of claim 62, wherein said means for comparing the

integrated amplified digital signal with a threshold comprising a training generator feeding at least one known digital signal to said input digital signal in a training period, and reading said known digital signal and digital result from at least one ADC connected to said at least one analog output signal, and identifying the model of said multi-stage digital signals constructor by applying a system identification algorithm.

67. The device of claim 66, wherein said training generator is implemented within said DSP.

68. A parallel multi-stage digital input constructor, comprising;

(a) plurality of digital input constructors receiving at least two different digital input signals,

(b) said plurality of digital input constructors are placed on the same silicon substrate, featuring crosstalk between said plurality of digital input constructors,

(c) a common DSP for treating said crosstalk effect,

whereby each stage of each multi-stage digital input constructor comprising: amplifier amplifying an input digital signal, integration means for integrating the amplified digital signal, a synchronization clock synchronizing said multi-stage digital input constructor, a comparator for comparing the integrated amplified digital signal with a threshold, and adding at least one predefined correction to said amplified digital signal.

69. A method for constructing at least one digital input signal and providing at least one analog representation signal thereof, comprising:

(a) feeding a DSP with said at least one digital input signal and a synchronization clock,

(b) said DSP is calculating n digital outputs, by using said at least one digital input signal and a model of said constructing device, whereby said model can be considered as having sufficient accuracy,

(c) said n digital outputs are received by k discrete output devices comprising, in total, n digital inputs, m analog outputs, and simple conversion rules between said n digital inputs and said m analog

outputs,

(d) said MIMO system receiving said m analog outputs, and providing at least one output analog signal equivalent to said al least one digital input signal.

70. The method of claim 69, wherein said sampler can be considered as time invariant by using analog or digital compensation methods.